

FIG 2

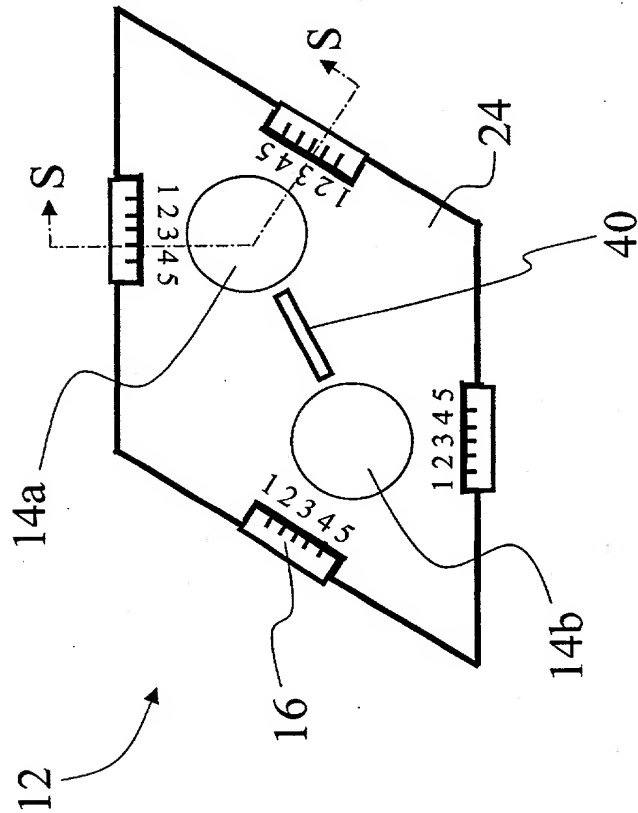


FIG 3

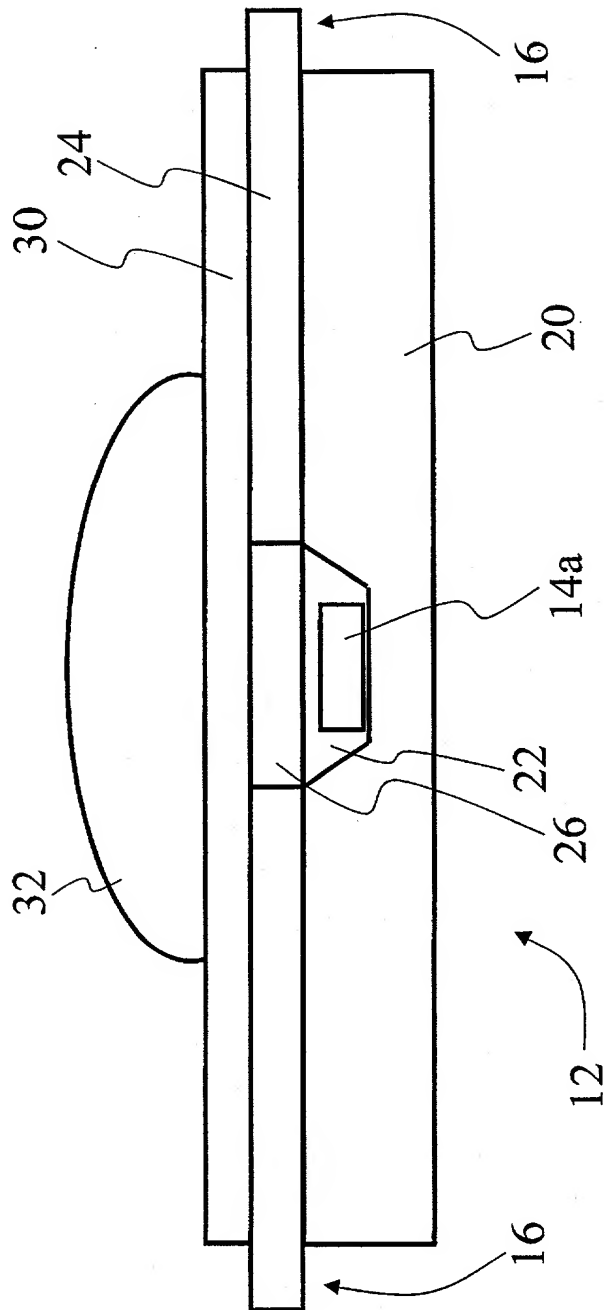


FIG 4

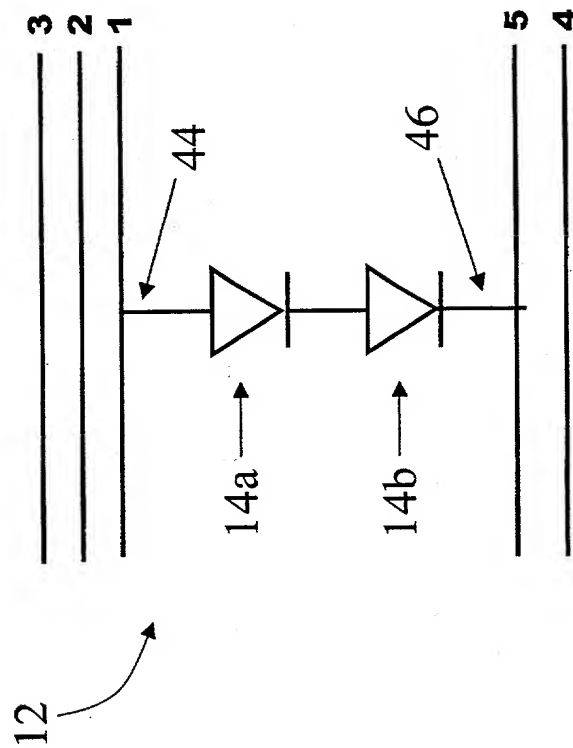
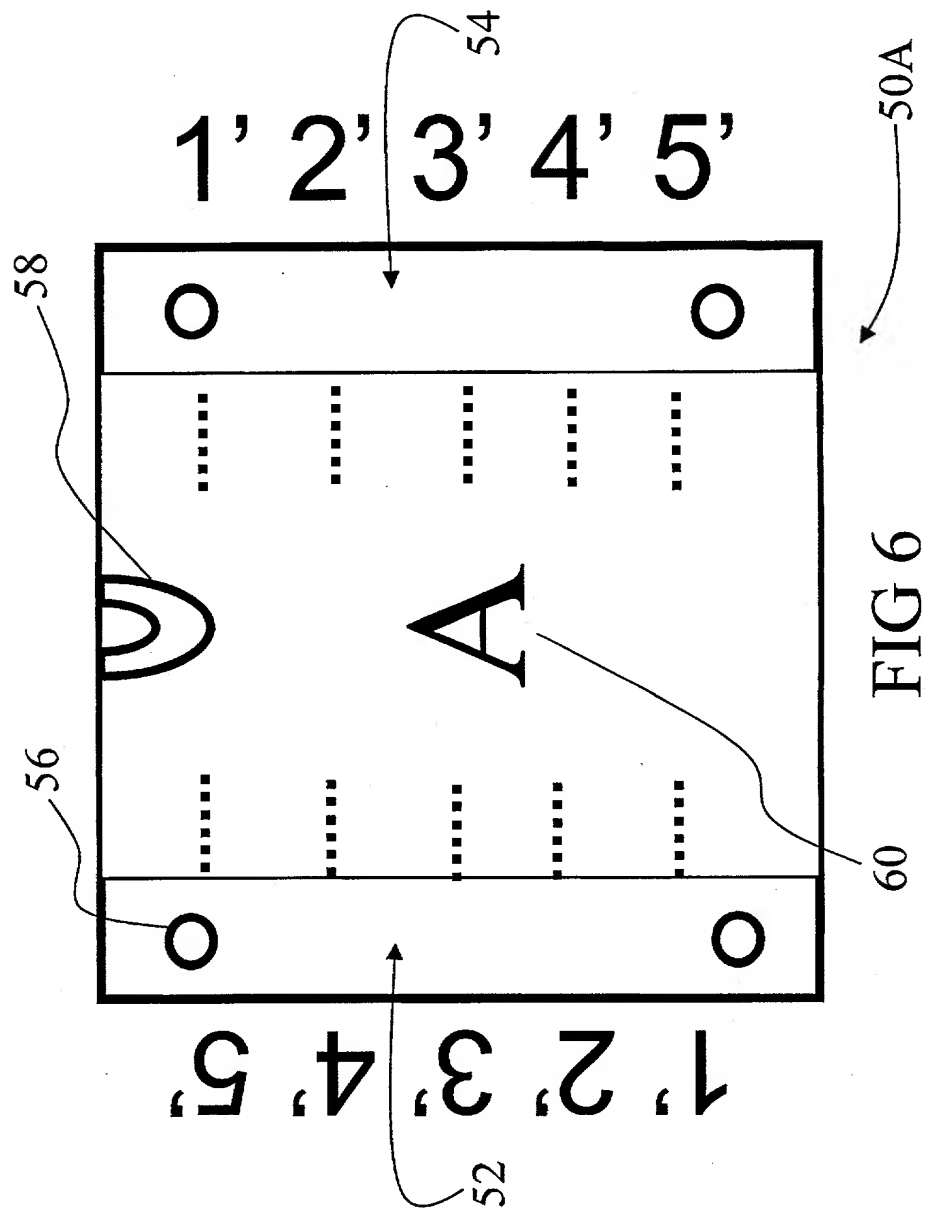


FIG 5



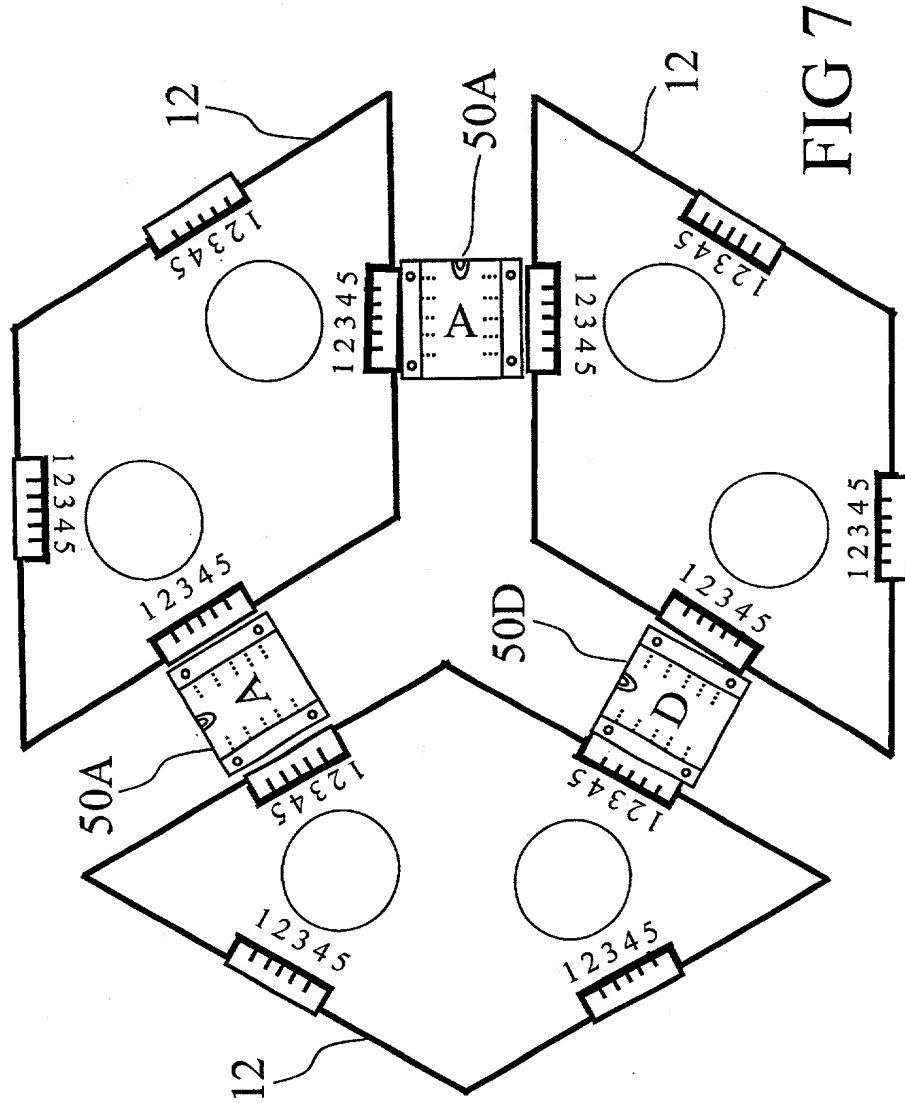


FIG 7

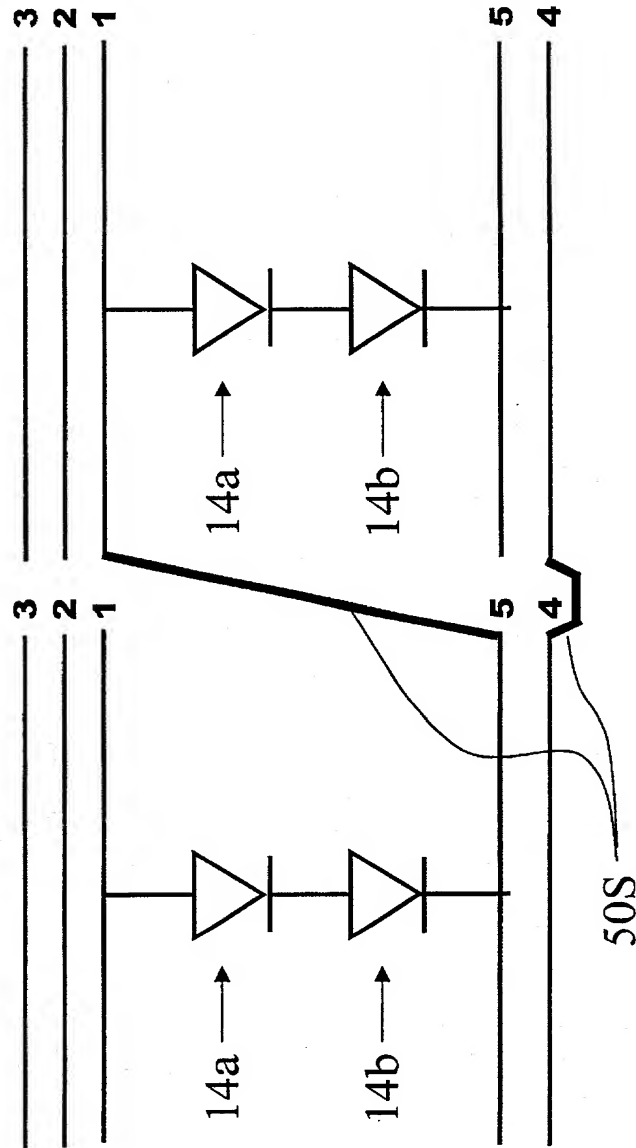
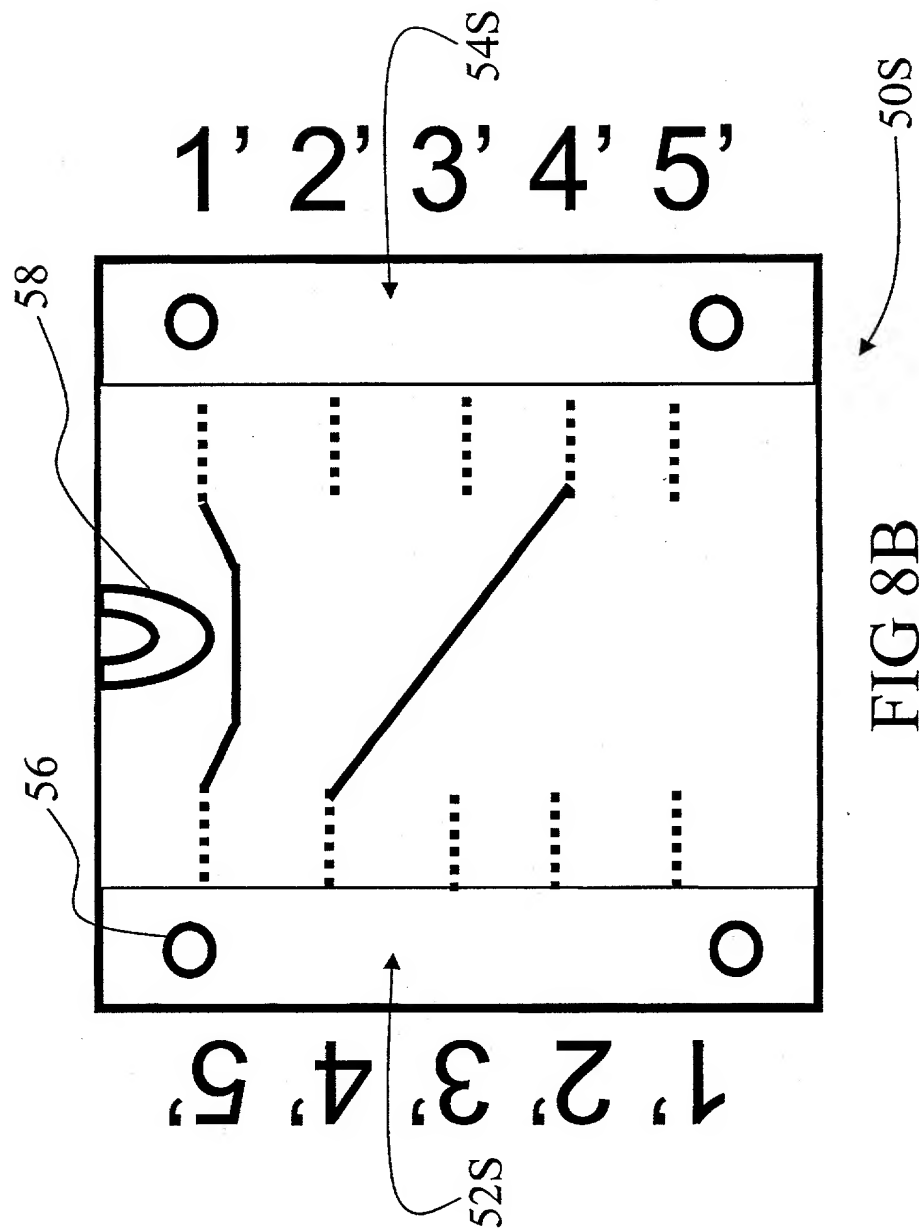


FIG 8A





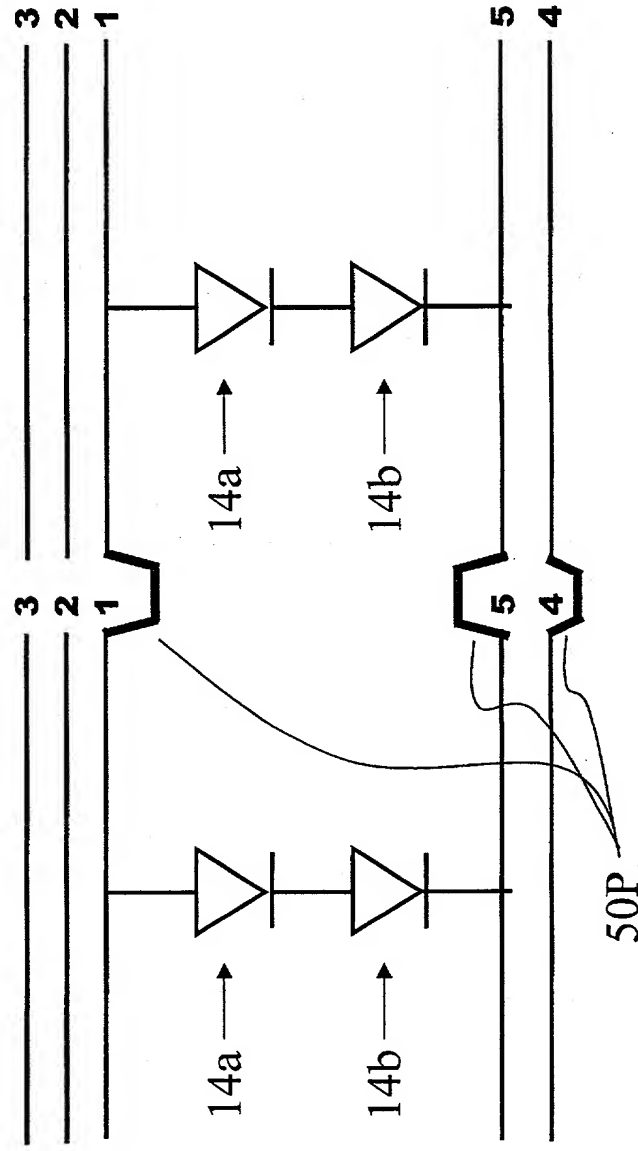
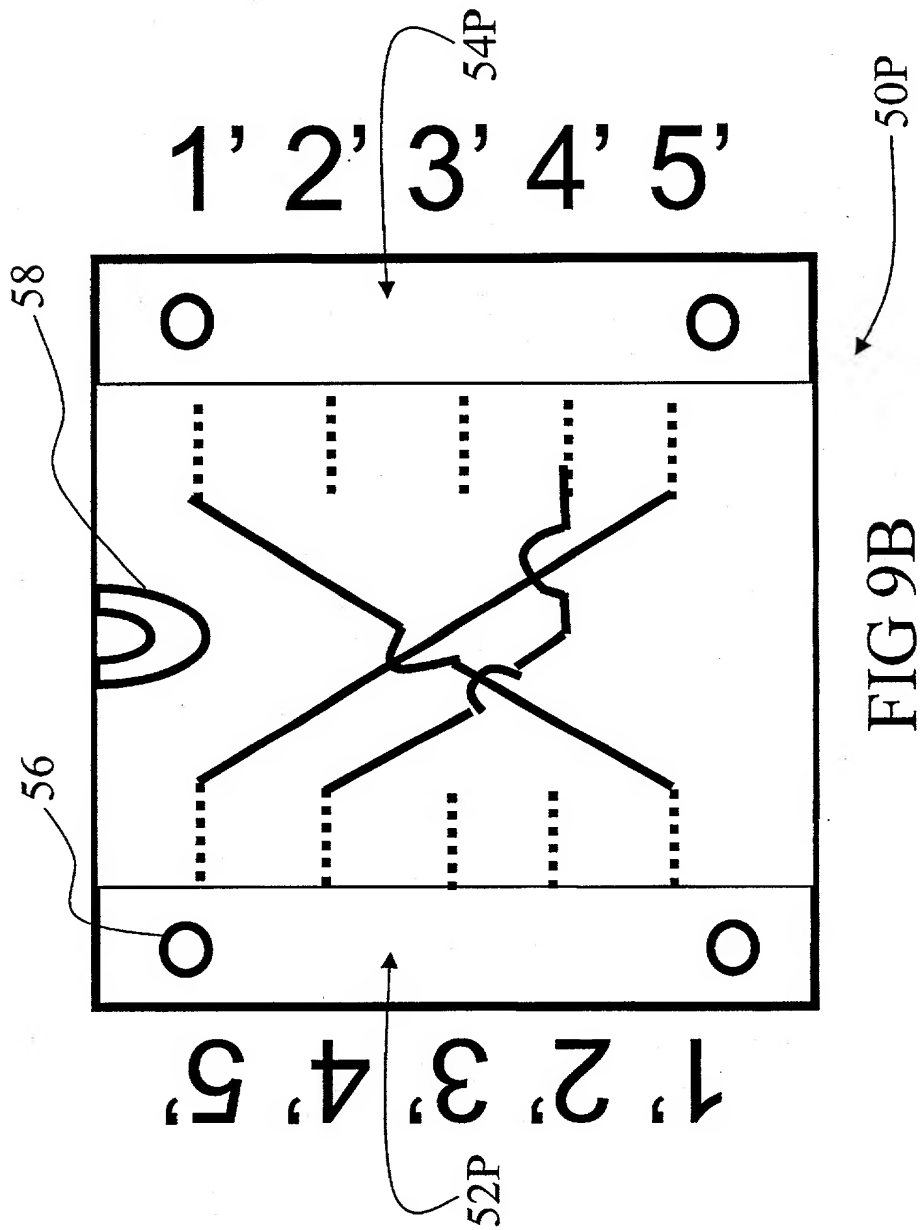
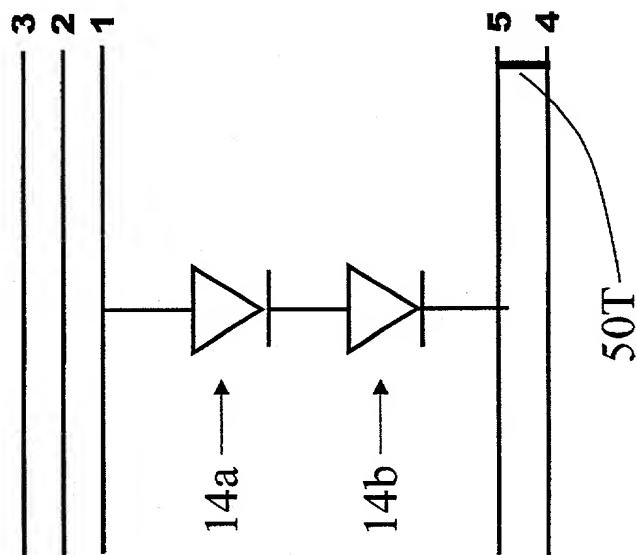


FIG 9A





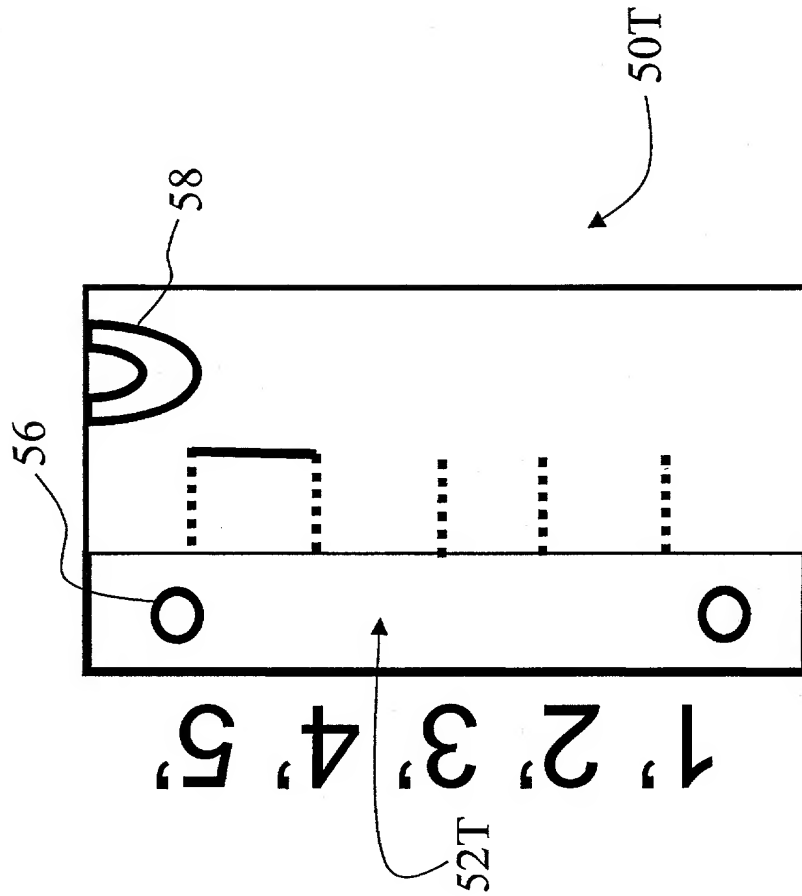


FIG 10B

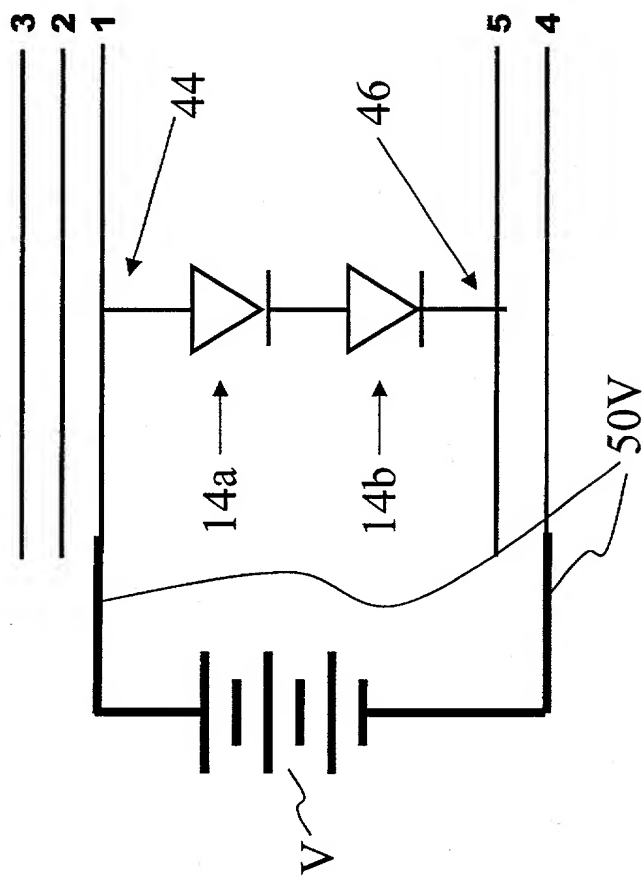


FIG 11A

FIG. 11B is a schematic diagram of a device 50. The device 50 includes a substrate 52 and a plurality of electrodes 54. The electrodes 54 are arranged in a row and are labeled 1', 2', 3', 4', and 5'. The electrodes 54 are connected to a voltage source 56. The voltage source 56 is connected to the electrodes 54 via a cable 58. The cable 58 is connected to a voltage source 64. The voltage source 64 is connected to the electrodes 54 via a cable 64.

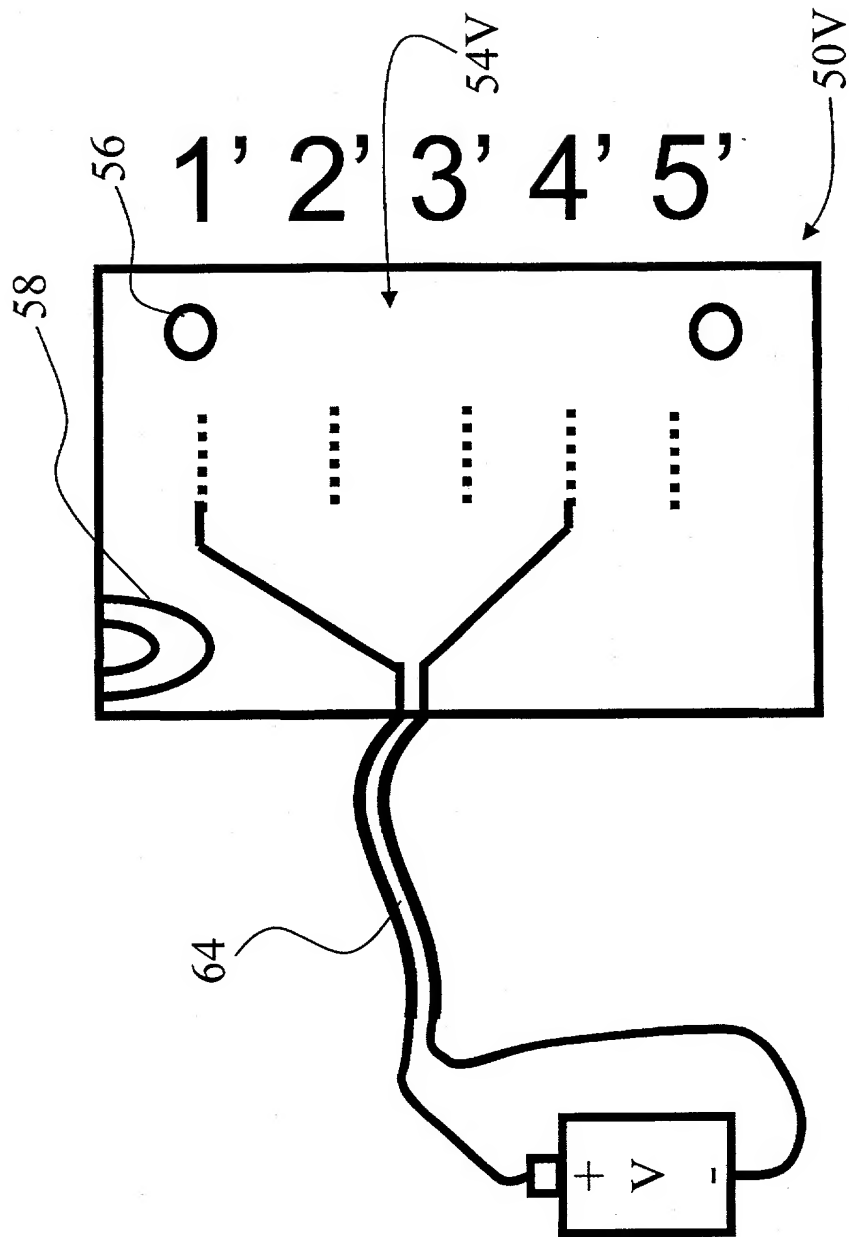
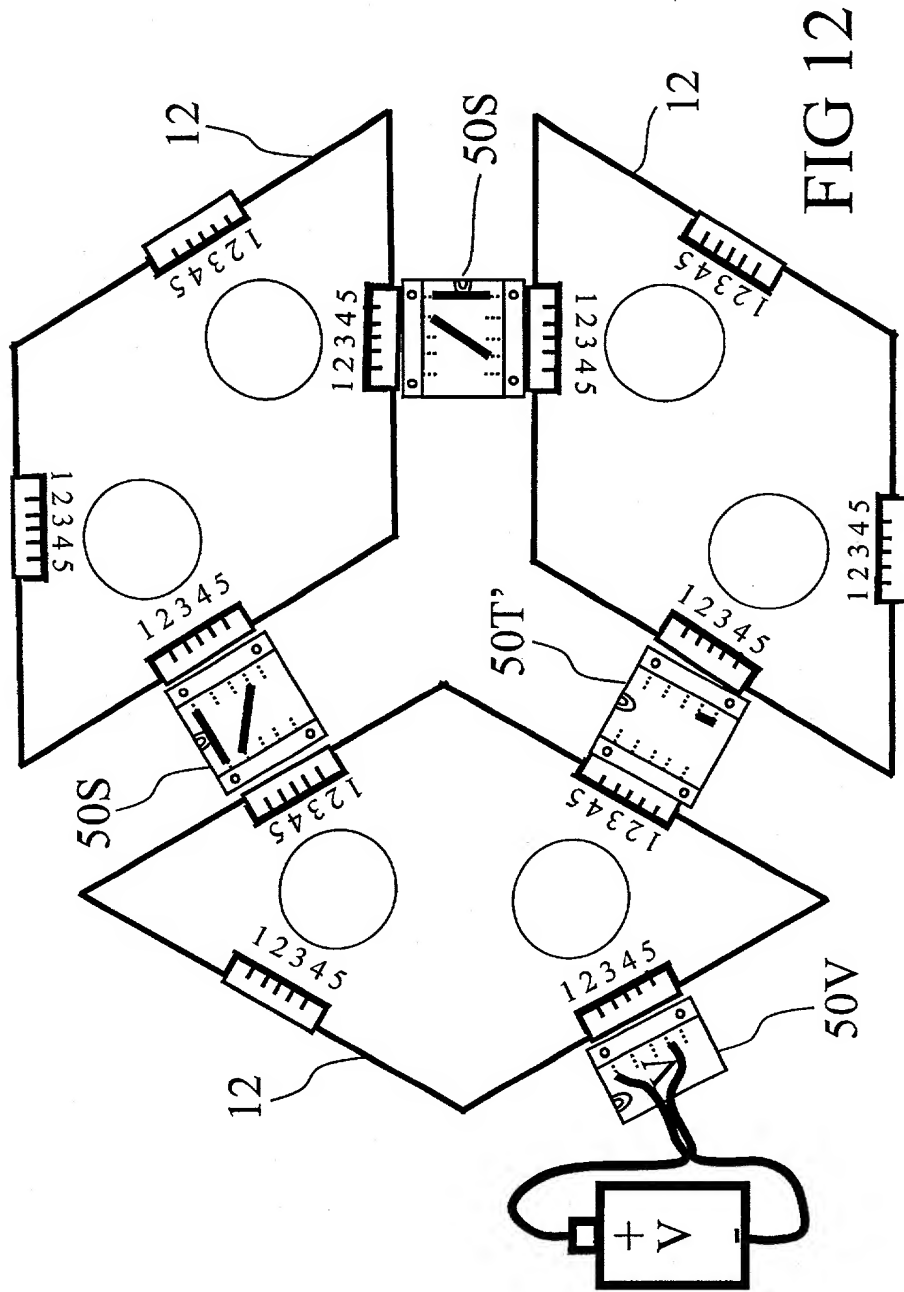


FIG 11B

FIG. 12 is a schematic diagram of a circuit for testing a device under test (DUT) 12. The circuit includes a power source 50V, a switch 50T, and a load 50S. The DUT 12 is connected to the power source 50V through the switch 50T and the load 50S. The circuit is configured to measure the current flowing through the DUT 12 and the voltage across the load 50S.





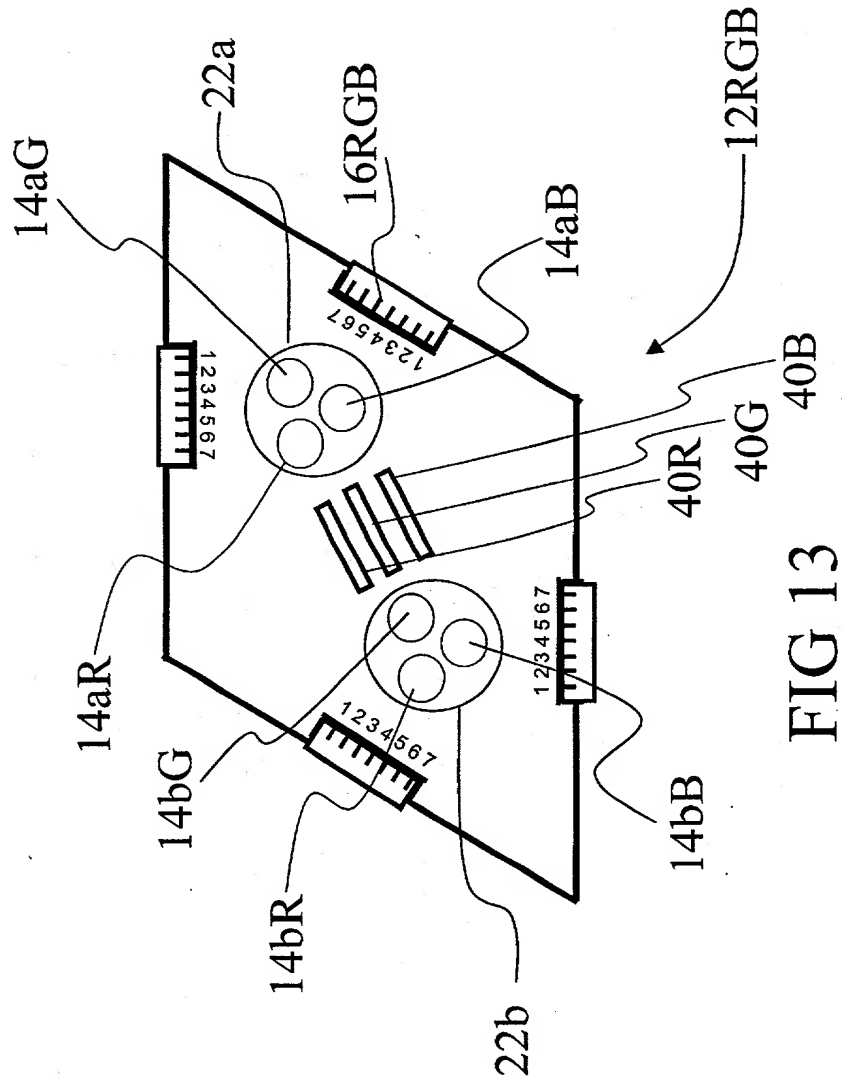


FIG 13

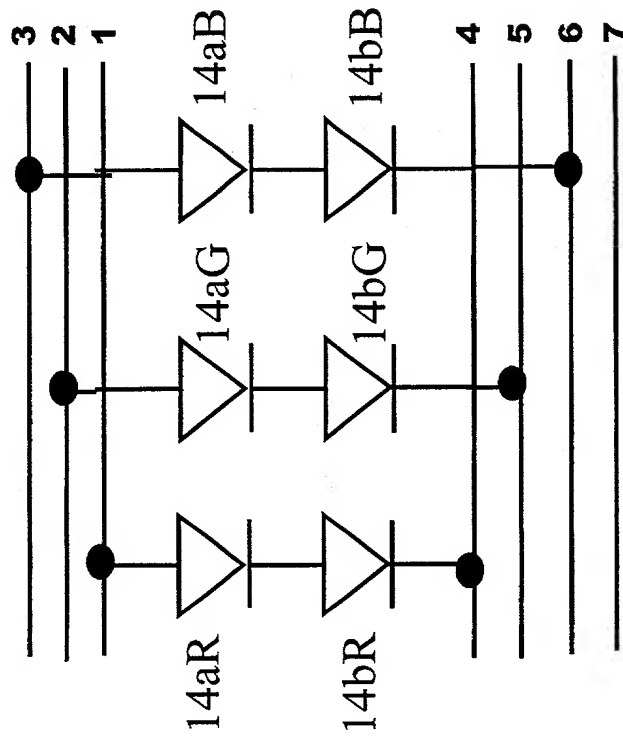


FIG 14

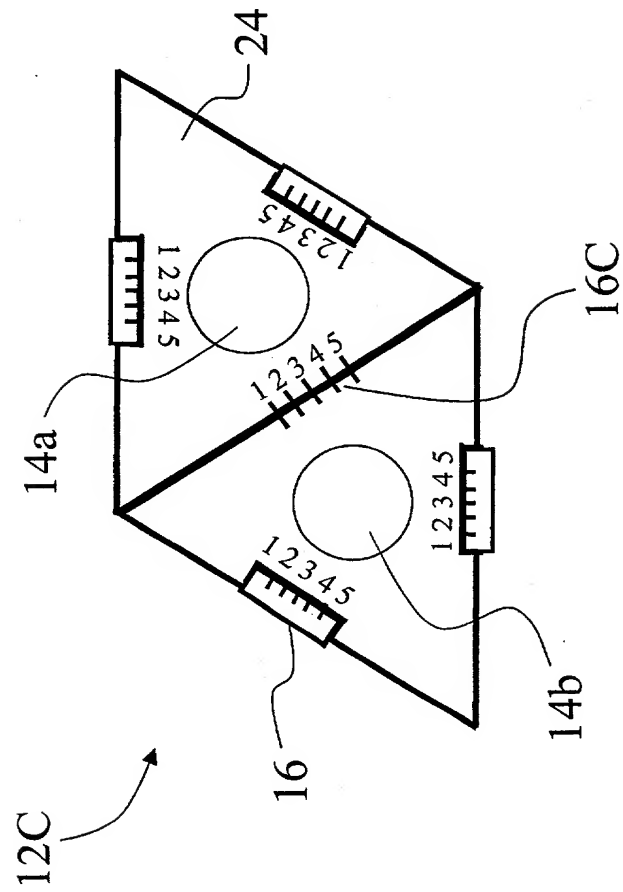


FIG 15

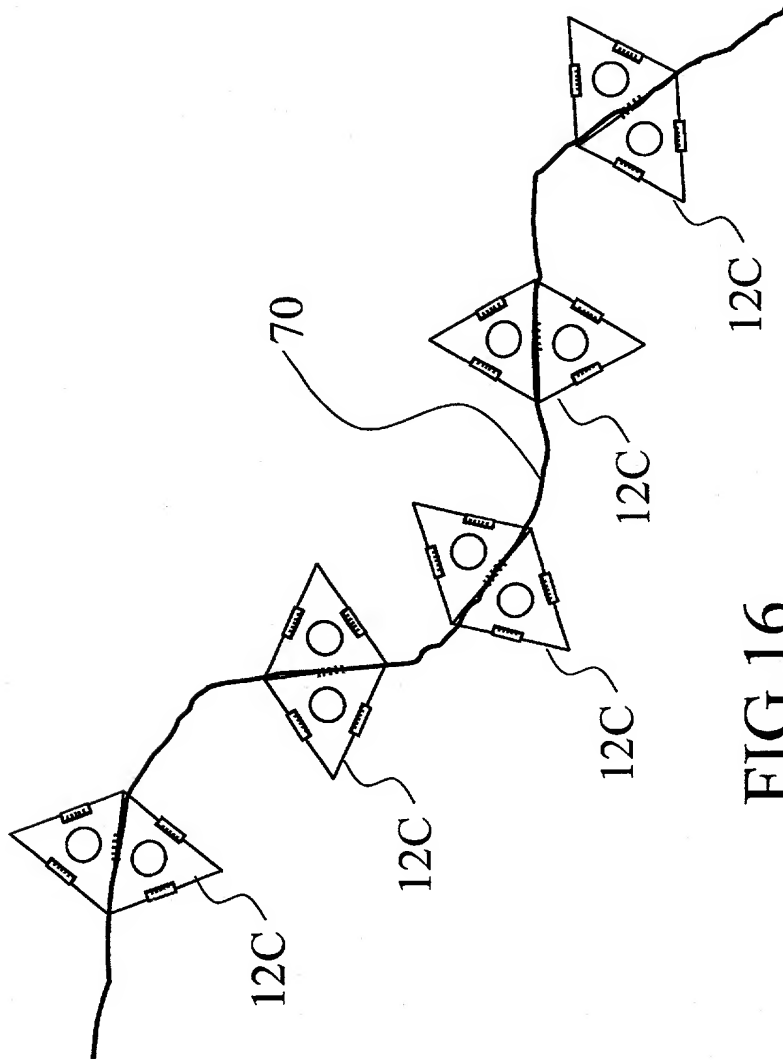


FIG 16